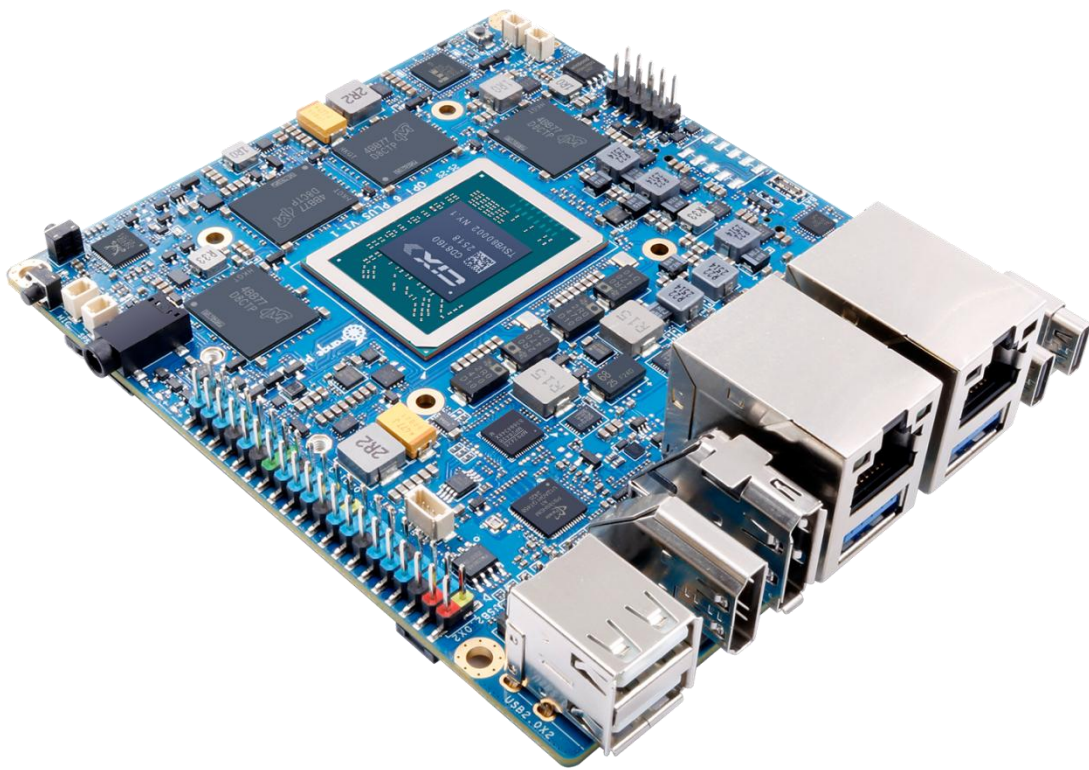




Orange Pi 6 Plus Bios User Manual





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1.BIOS data address

Reference website for BIOS release package and user manual:

<http://www.orangepi.org/html/hardWare/computerAndMicrocontrollers/service-and-support/Orange-Pi-6-Plus.html>

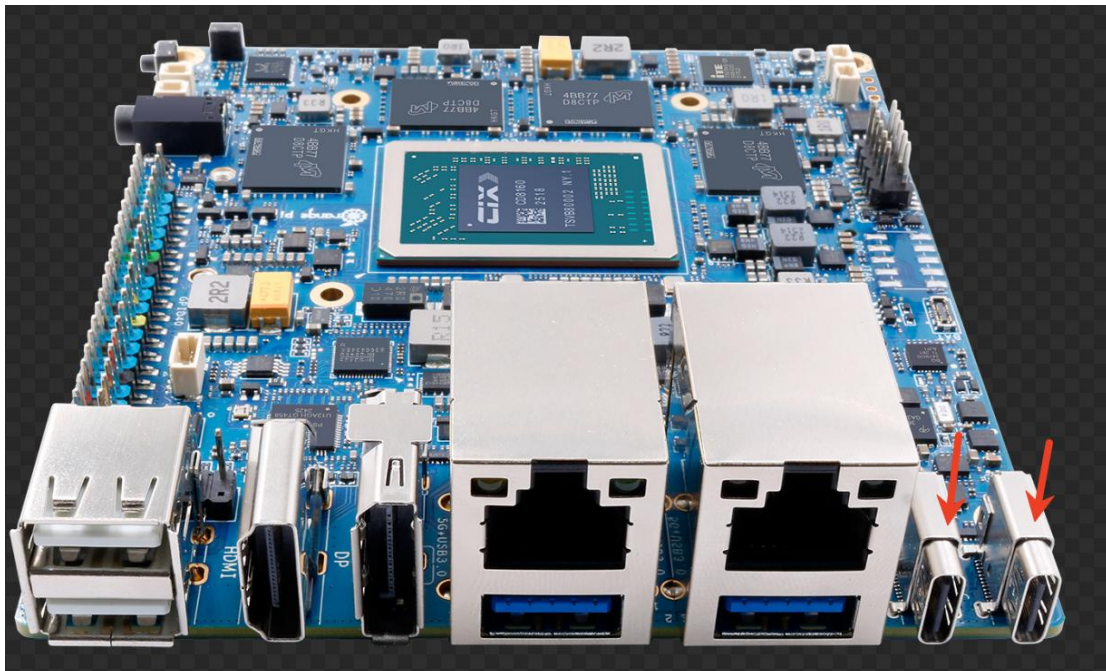
Click on the "User Manual" icon on the official website page to access BIOS related manuals

Click on the "BIOS" icon on the official website page to download BIOS firmware, etc., and use it in conjunction with the manual

2.Power On

2.1 Power on

Both Type-C interfaces of the development board can be used for power supply

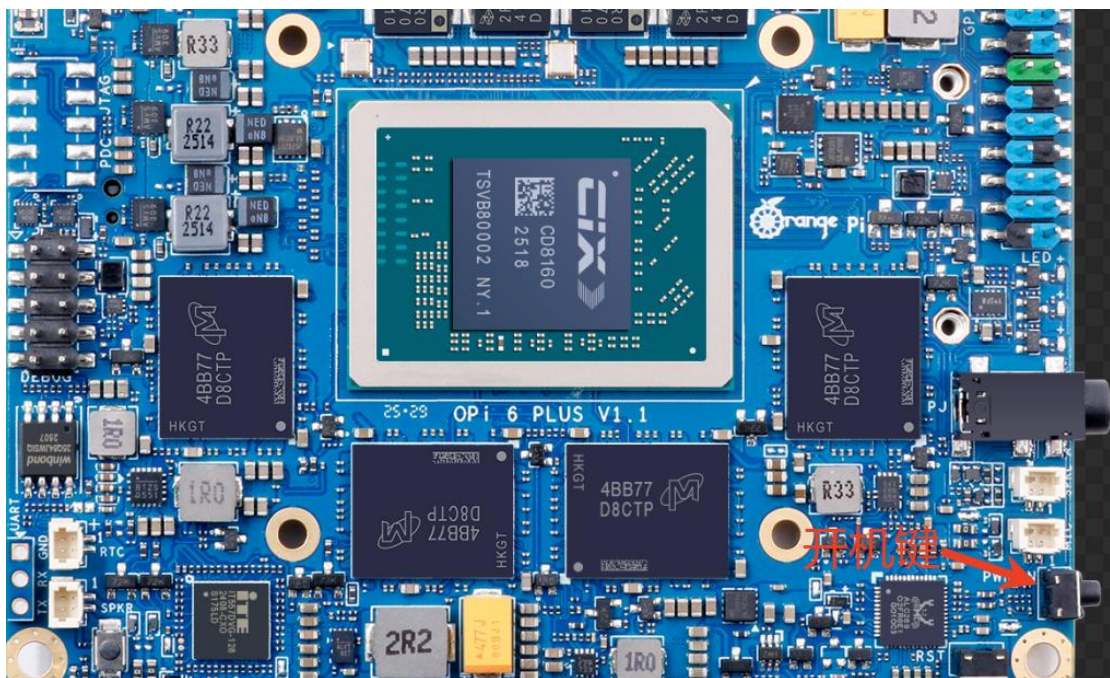


Currently using a 100W 20V PD power adapter



2.2 Enter BIOS SETUP Menu

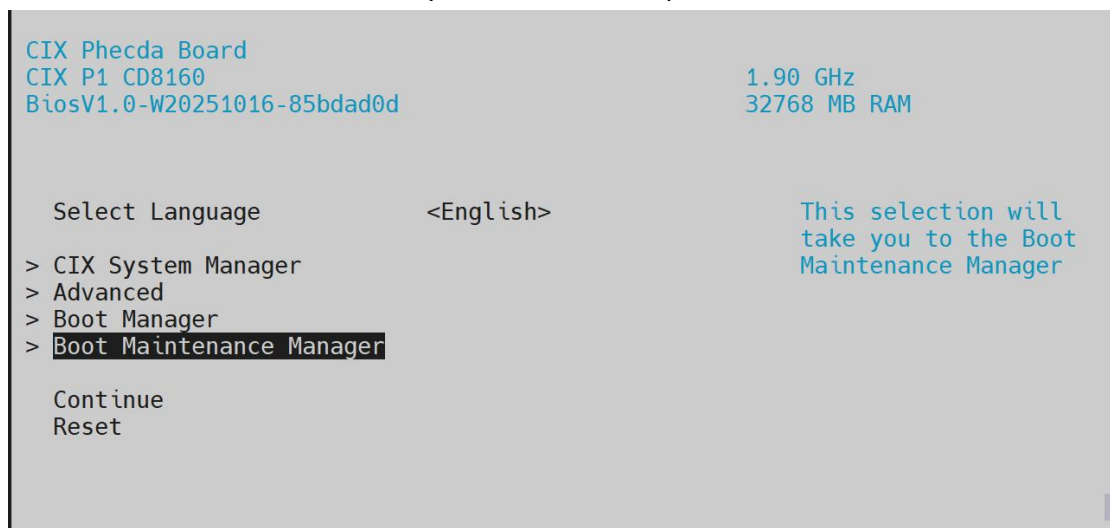
1) Connect the development board to the screen and keyboard, power on, and press the power button to turn on the device.



The interface for loading the logo is shown in the following figure:



2) Press the F2/ESC shortcut key to enter the setup interface as follows



2.3 LED light

There are 3 LED lights on the Orange Pi 6 Plus board.

Green light: After connecting the power adapter and pressing the power button, the green light flashes; When sleeping, the green light stays on constantly; After shutting down, the green light goes out

Blue light: After connecting the power adapter, the blue light will turn on.

Red light: Connect the battery, and when the battery is charging, the red light flashes; When the battery is fully charged, the red light remains on; When powered solely by batteries, the red light remains on When the battery is removed, the red light goes out



3.SETUP interface

3.1 User Interface (UI) Design

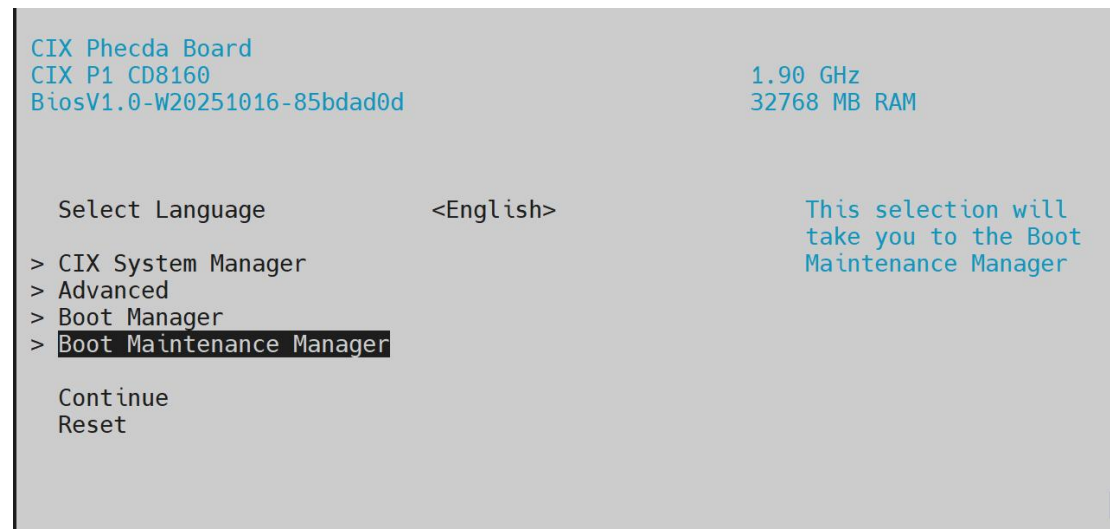
Bios compilation time

CPU Name

Start frequency

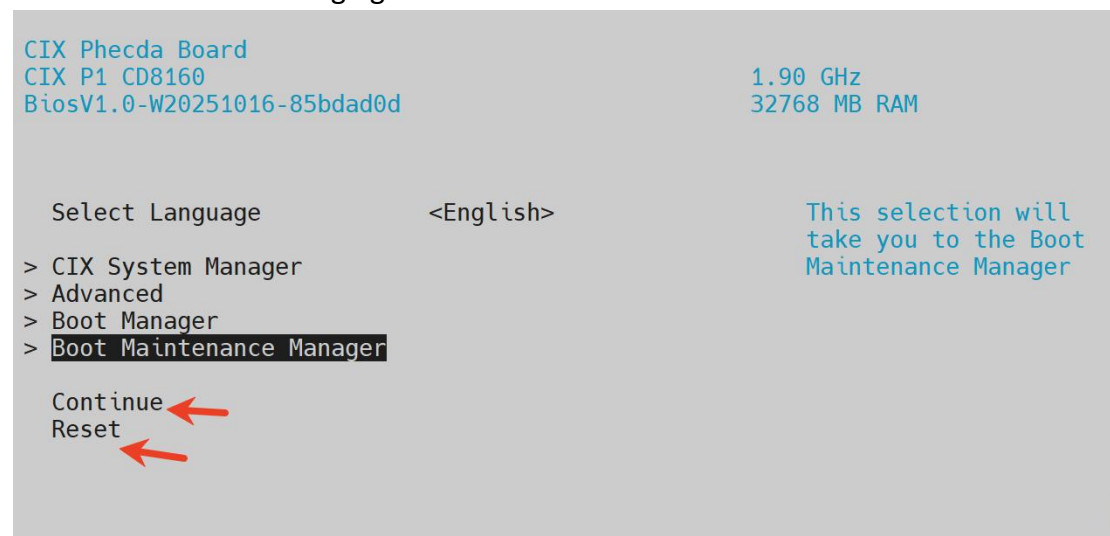
DDR capacity

as shown in the figure below



3.2 Continue/Reset

As shown in the following figure:



After pressing the Continue option, if an SSD hard drive is connected, the system will

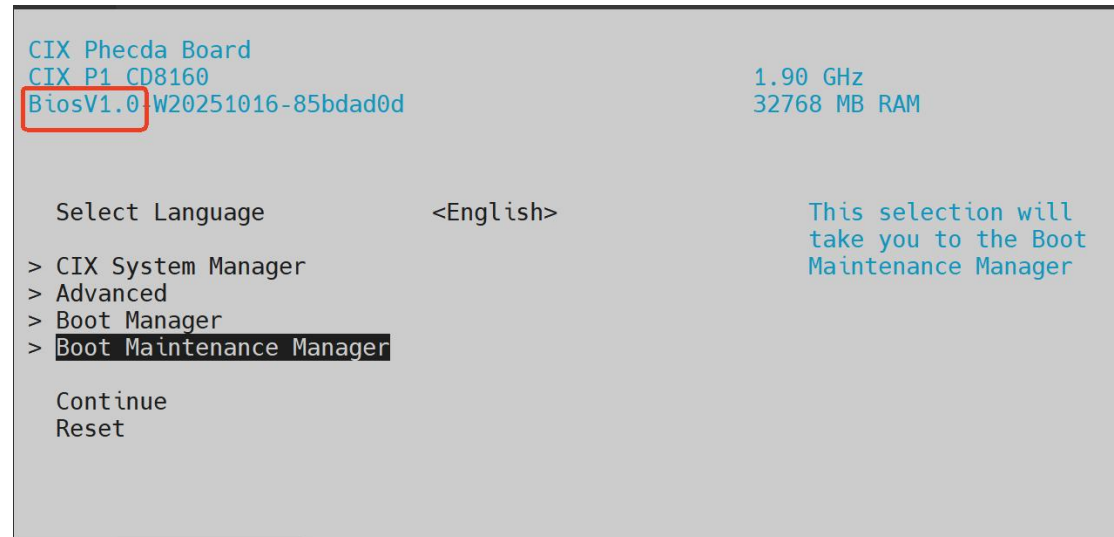


continue to enter the hard drive.

After pressing the Reset option, the development board will restart.

3.3 Version Information

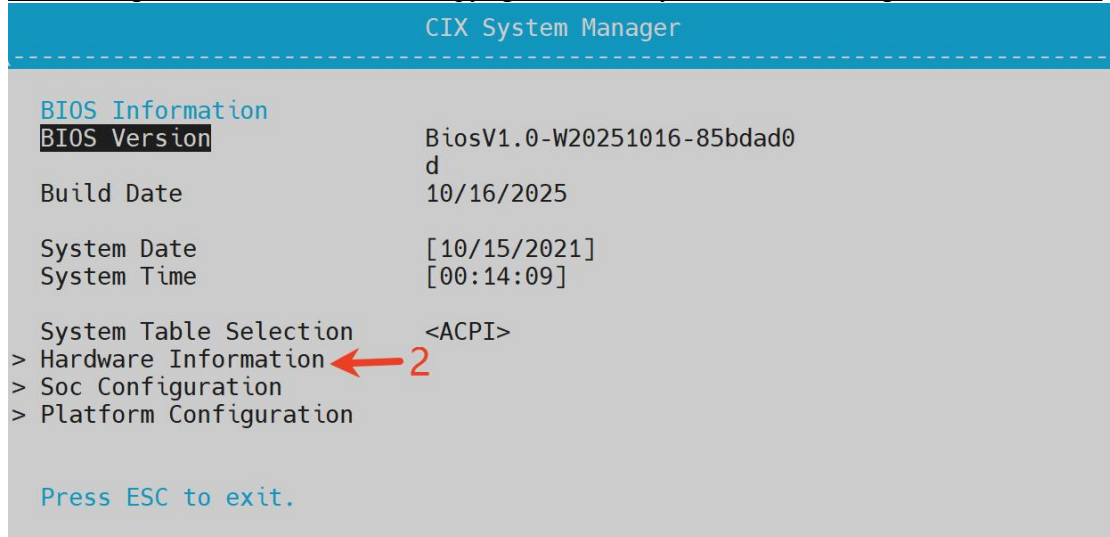
Bios version information



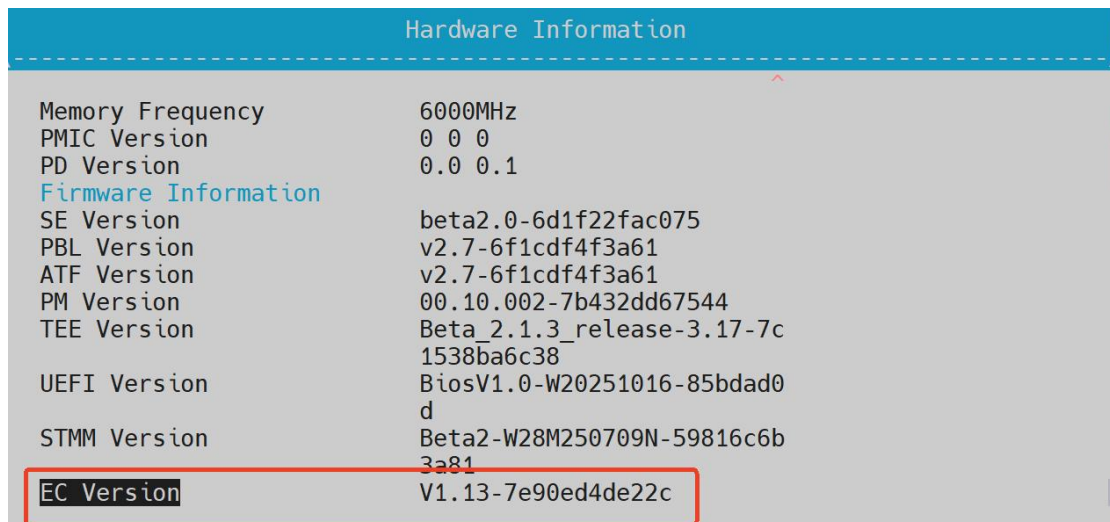
EC version information

The EC version information option displays the path under Cix System Manage->Hardware Information.





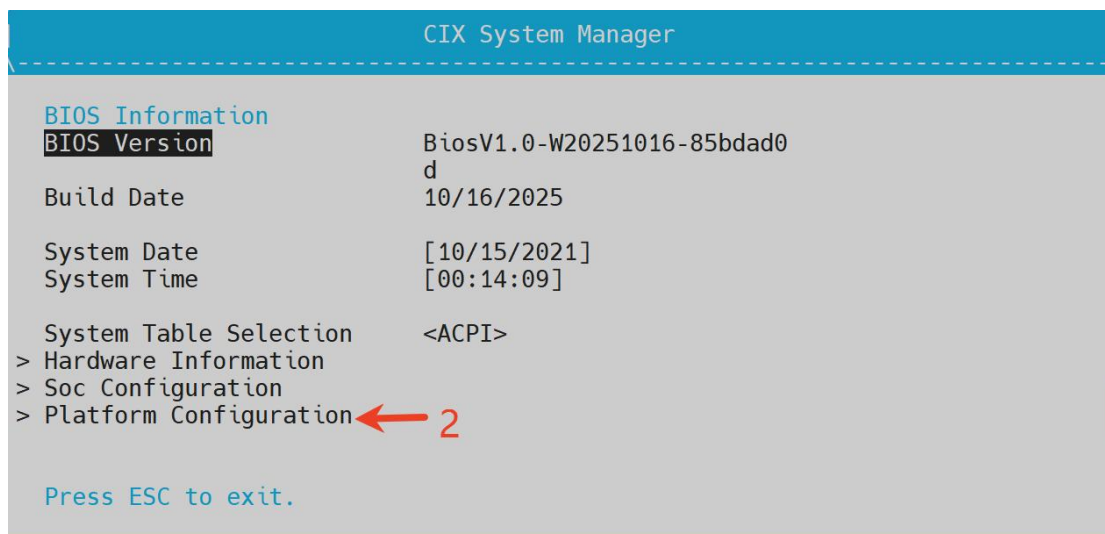
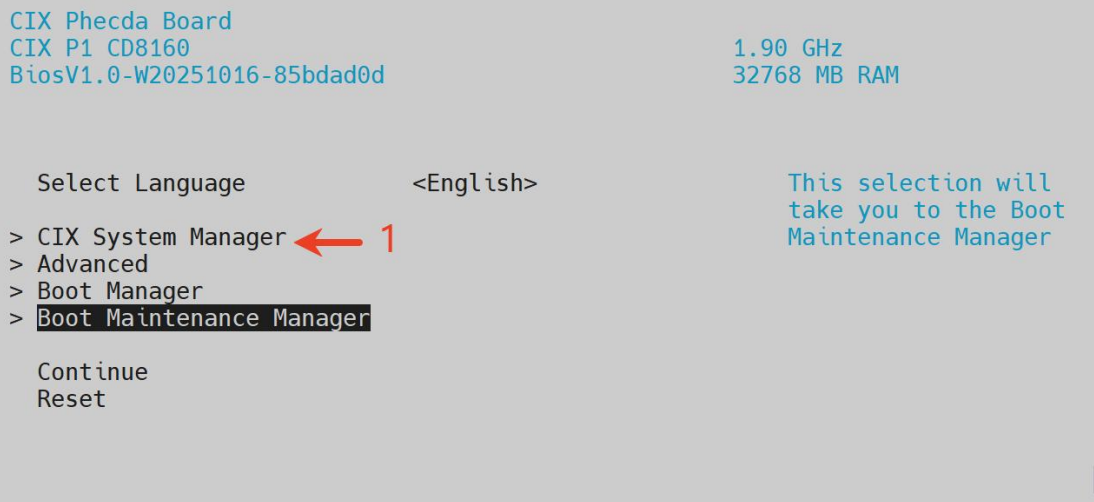
The EC version information is shown in the following figure:



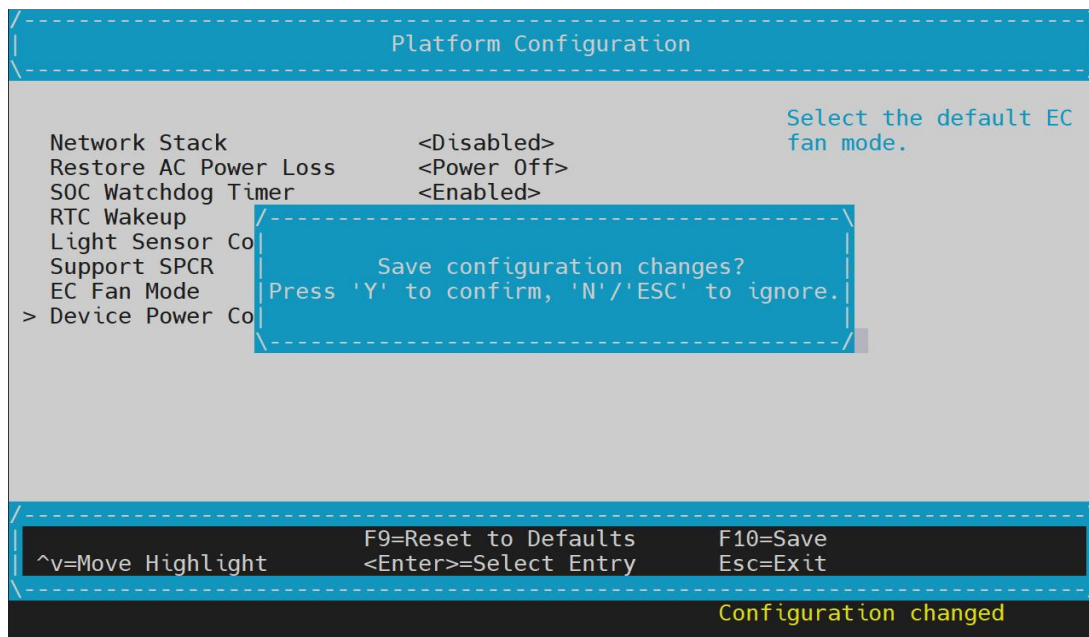
3.4 Option Save

Option Save: Use the F10 shortcut key to save and restart the board to take effect. For example, change the EC fan mode option to performance mode and press the F10 shortcut key to save the data.

EC fan mode option path: Open Cix System Manager -> Platform configuration



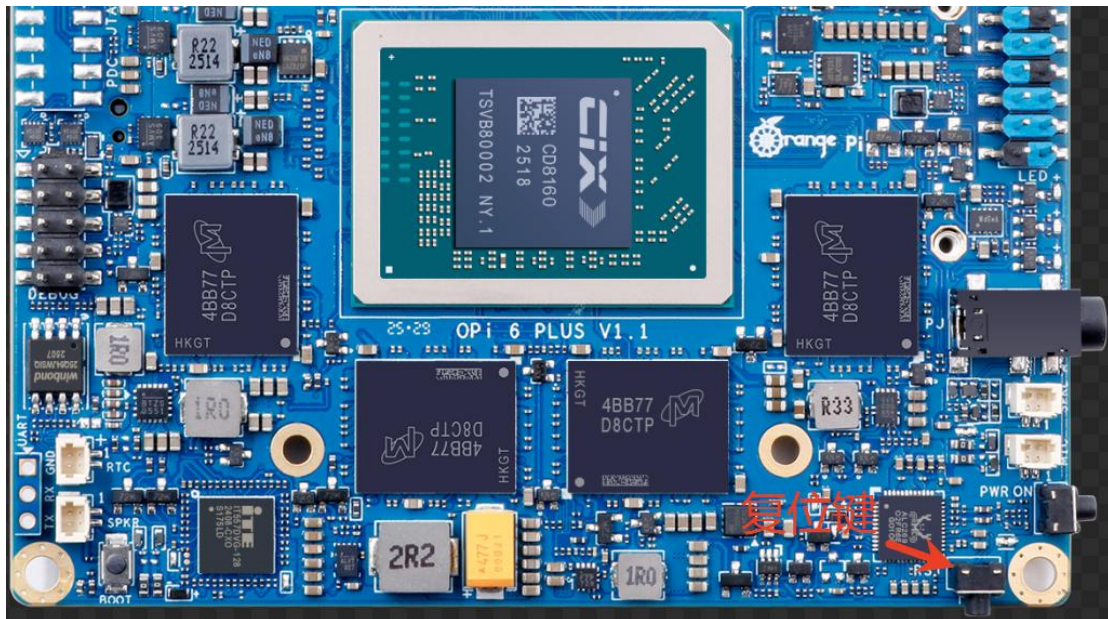
Press the F10 shortcut key, as shown in the following figure:



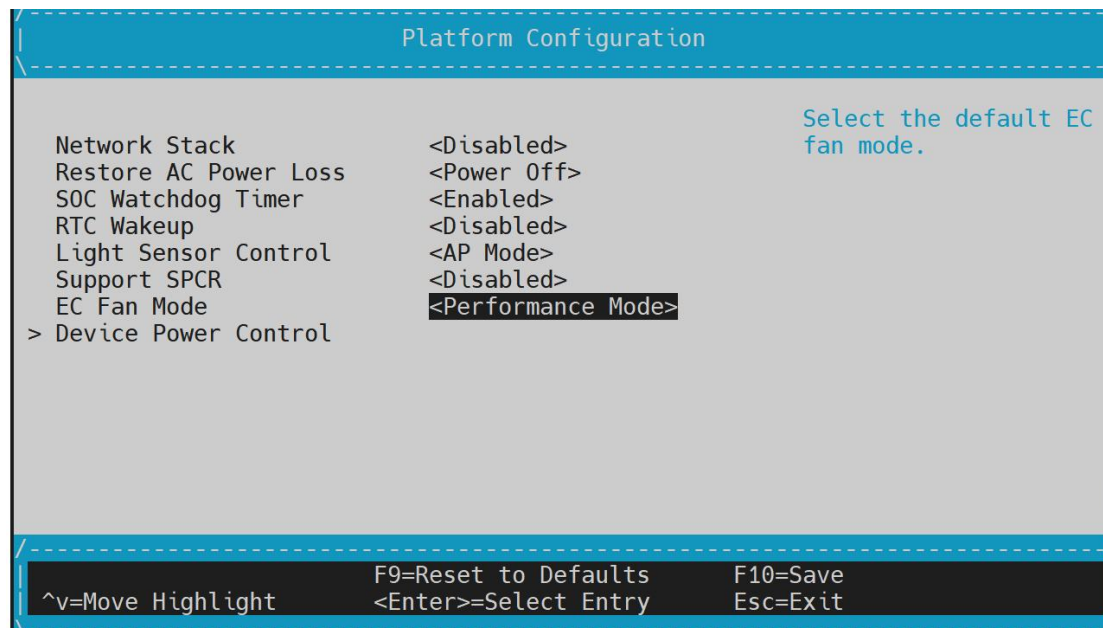
Press Y on the keyboard to confirm.



Then press the reset button to restart the development board.



Re enter the BIOS interface, where the EC Fan Mode has been changed to Performance Mode, indicating that the option has been successfully modified. 进入 BIOS



Note: Modifying options requires keeping the power adapter connected in order to prevent data loss; Or connect an RTC button battery to save BIOS data.

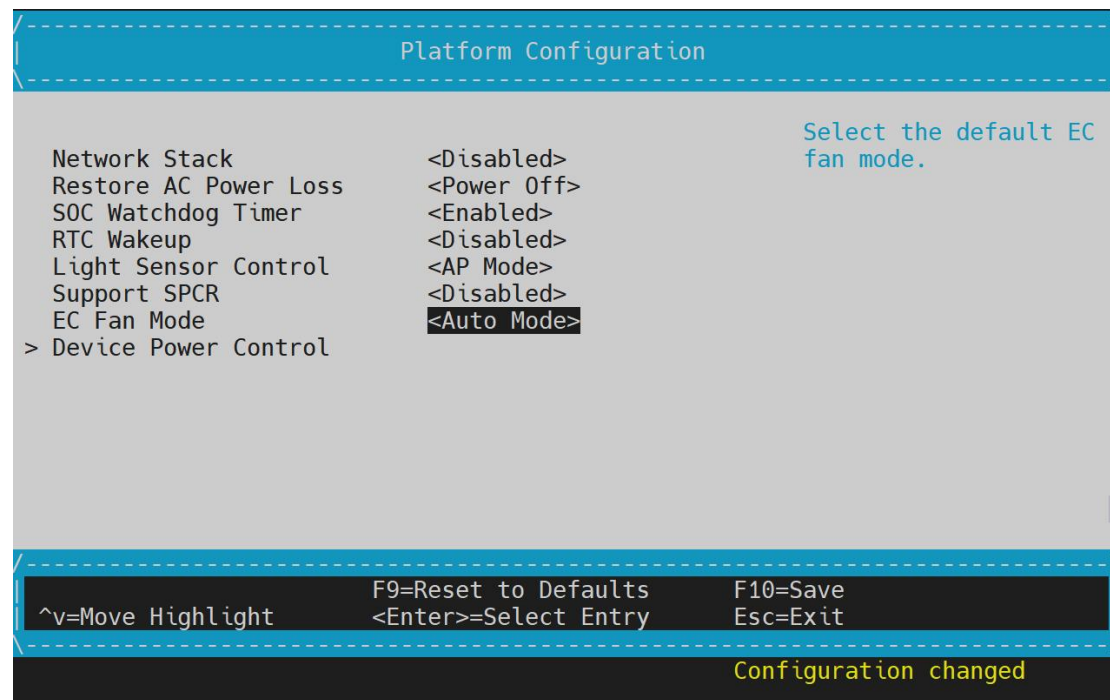
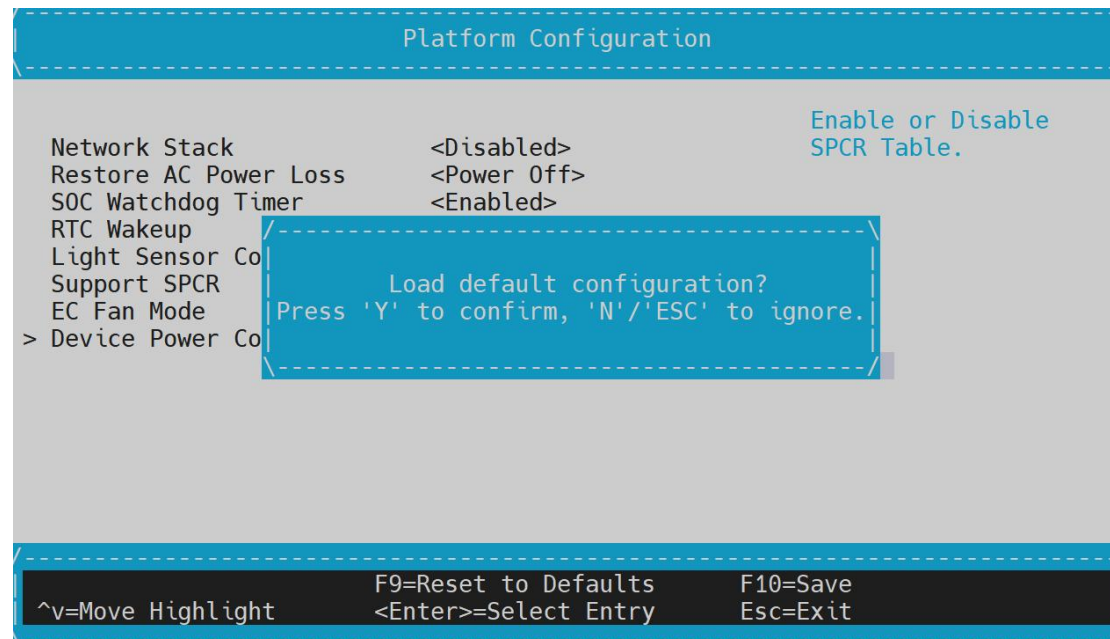


3.5 Load default configuration

Default option loading: Press F9 to restore default settings, then press F10 to save and restart the board to take effect.

Scenario: When the user modifies the wrong option and wants to restore the default value.

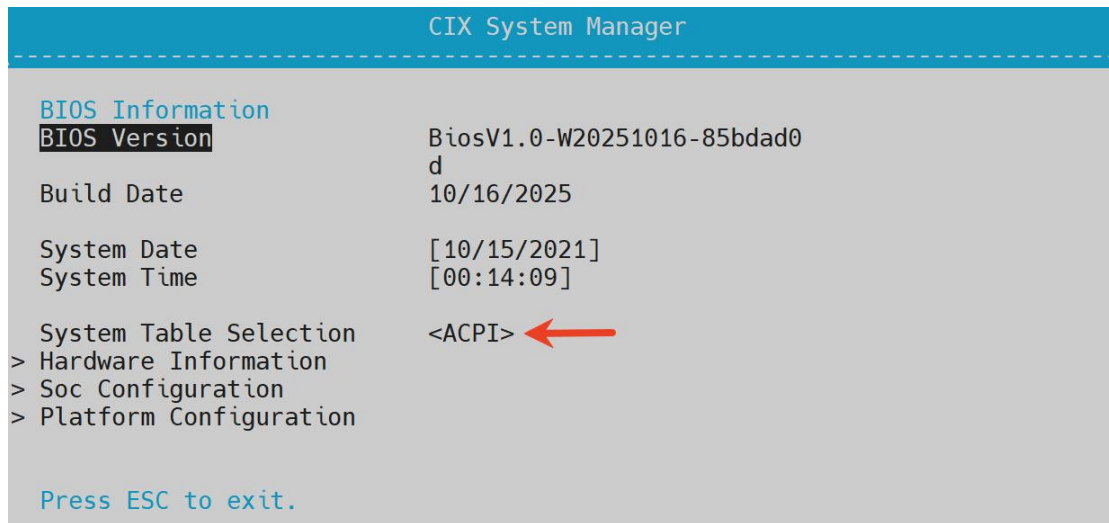
Press the F9 shortcut key and click Y to confirm.



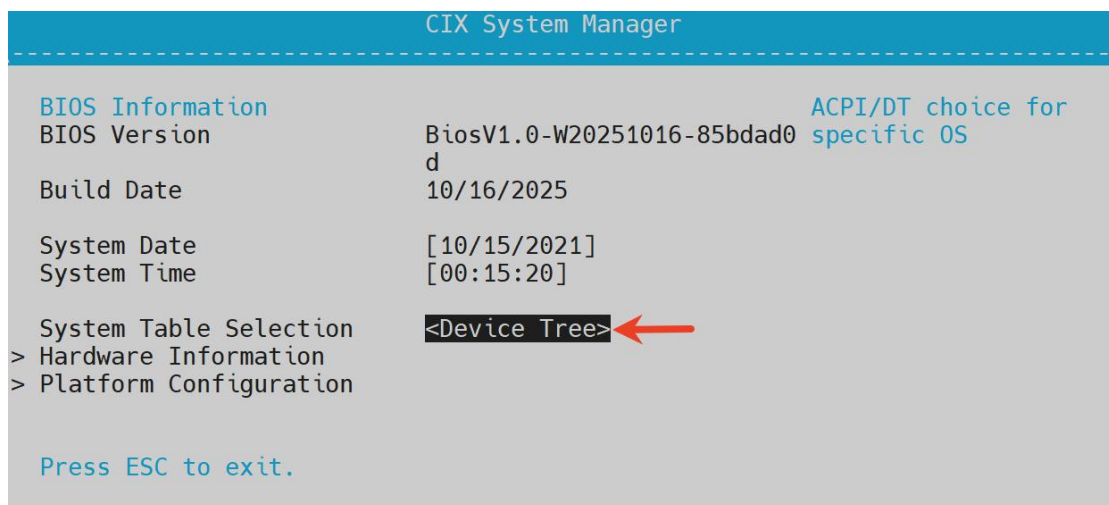
After restarting the board, the default values loaded will take effect.



3.6 Cix System Manage



System Table Selection: ACPI and Device Tree, When selected as Device Tree, Soc Configuration will be hidden.



3.6.1. Hardware Infomation

This interface displays the firmware version information and its contents.



```
CIX Phecda Board
CIX P1 CD8160
BiosV1.0-W20251016-85bdad0d

1.90 GHz
32768 MB RAM

Select Language      <English>
This selection will
take you to the Boot
Maintenance Manager

> CIX System Manager ← 1
> Advanced
> Boot Manager
> Boot Maintenance Manager

Continue
Reset
```

```
CIX System Manager

-----

BIOS Information
BIOS Version      BiosV1.0-W20251016-85bdad0d
Build Date        10/16/2025
System Date       [10/15/2021]
System Time       [00:14:09]
System Table Selection <ACPI>
> Hardware Information ← 2
> Soc Configuration
> Platform Configuration

Press ESC to exit.
```

This interface displays the firmware version information and its contents.

```
Hardware Information

-----

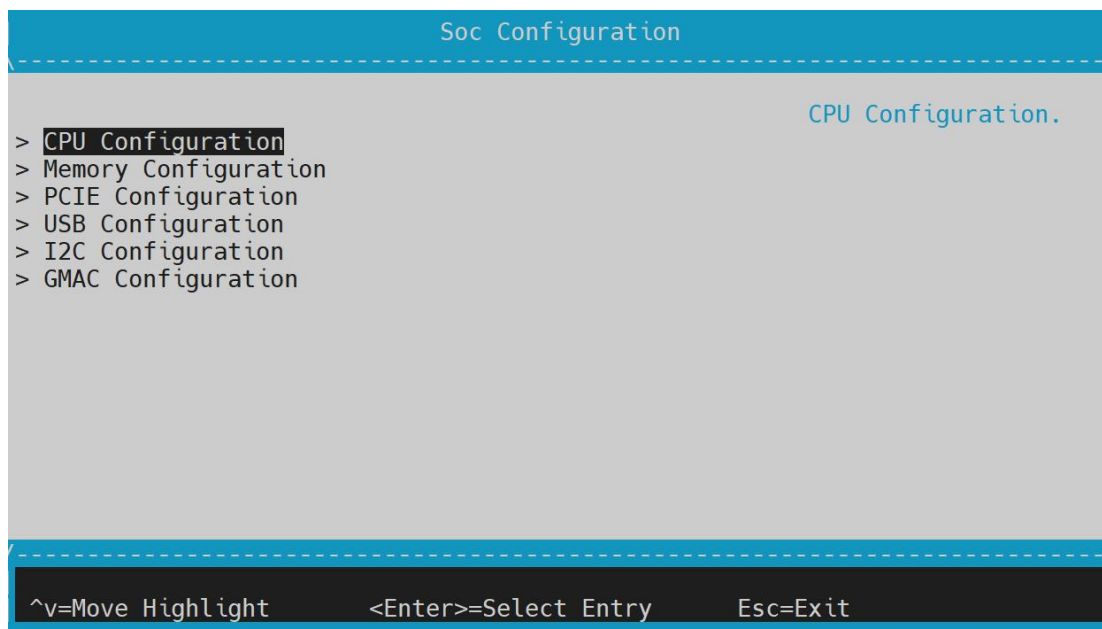
Hardware Information
Total Memory      32GB ← 内存容量信息
PCB SKU          PHECDA
Board Revision    Rev A
Memory Chip       Undefined
PMIC Version      0 0 0
PD Version        0.0 0.1
Firmware Information
SE Version        beta2.0-46f56d10502e
PBL Version       v2.7-2d3013792955
ATF Version       v2.7-2d3013792955
PM Version        00.10.002-b66f764a9452
TEE Version       Beta_2.0.3_release-3.17-6d
                  c7ab48a9ef
```



3.6.2. Soc Configuration

This interface is for Soc related configurations, such as CPU, memory, PCIE, USB, I2C, GMAC, etc.

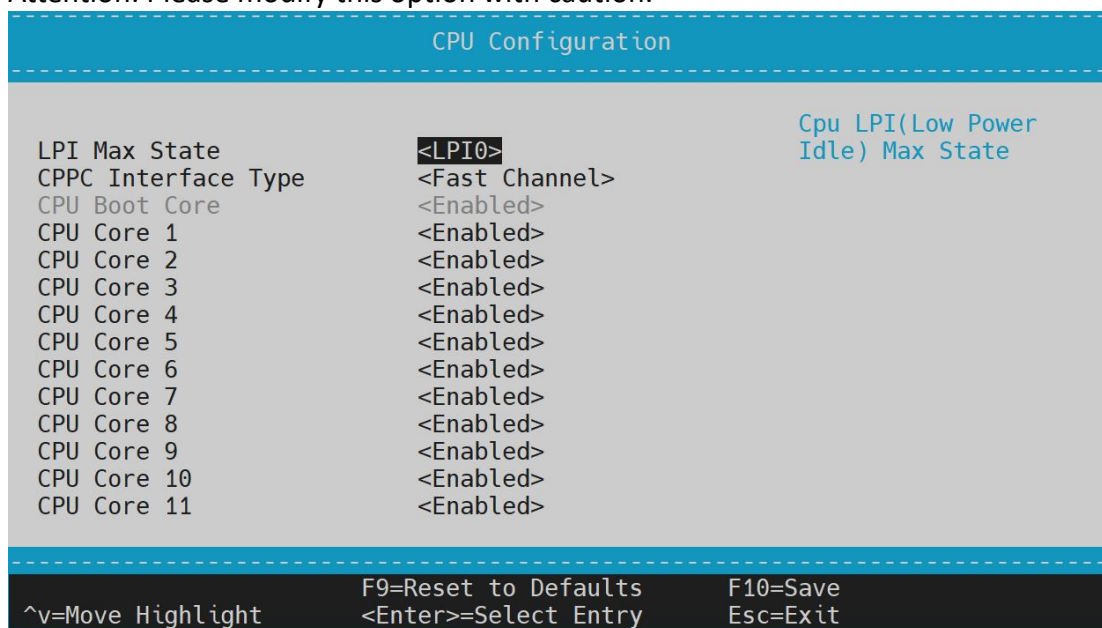
GMAC currently does not support the option of not requiring a career



3.6.3. CPU Configuration

This interface is the CPU's Core enable control switch.

Attention: Please modify this option with caution.

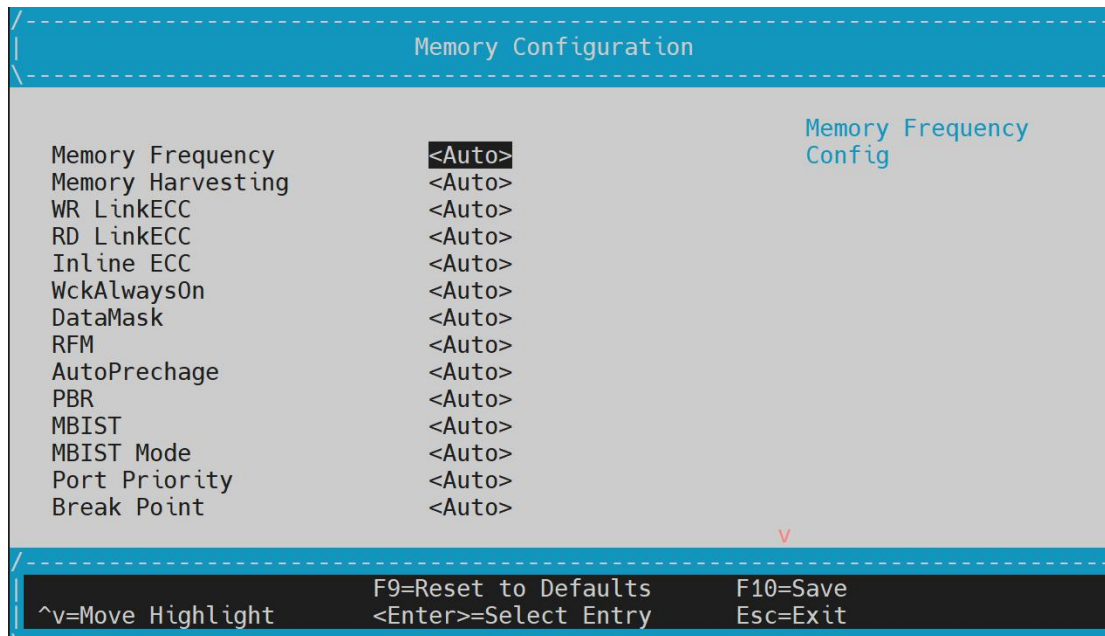




3.6.4. Memory Configuration

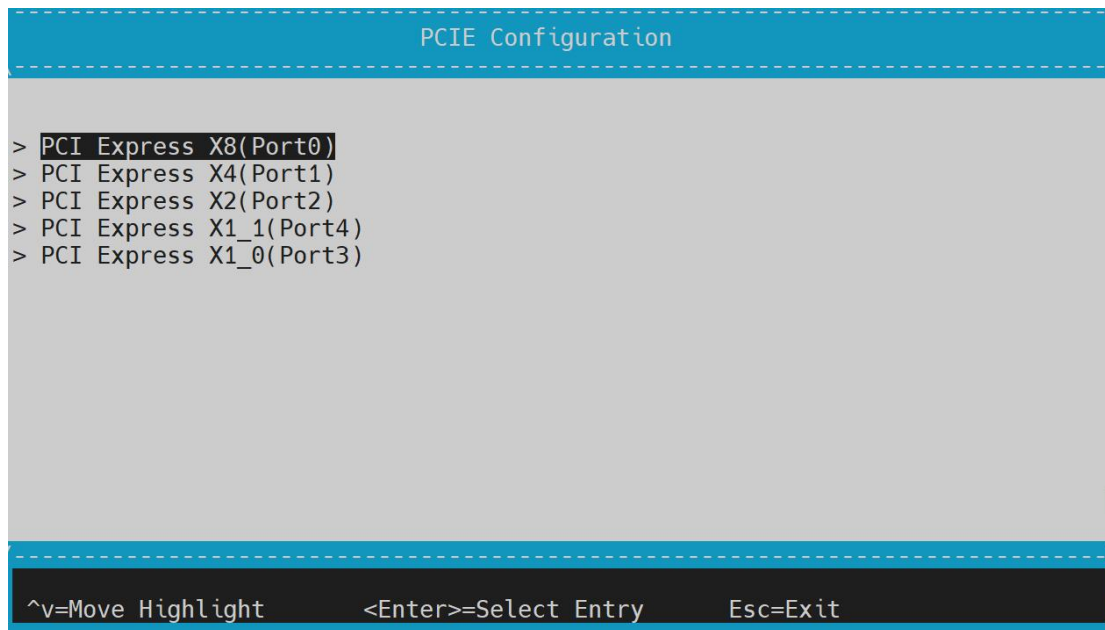
This interface displays relevant memory information configuration.

Attention: Please modify this option with caution.



3.6.5. PCIE Configuration

This interface is used to control the function setting switch of PCIE Port 0-4.



PCI Express x8(Port0): When the option is enable, enable the Pci root port 0, which is the SSD1 slot.

When the option is disabled, disable the Pci root port function.



PCIe Bandwidth:When the option is x4, set the PCIe bandwidth to x4.

PCIe Max Speed:When the option is Gen4, configure it to the maximum speed of Gen4.

Max Payload Support:When the option is 512 Bytes, set the maximum byte size of the Payload to 512 bits.

ASPM:This feature is not supported and does not require modification.

DTI Support:Support this feature, no modifications are required.

Note: Except for PCI Express x8(Port0), which can be modified and enabled, please keep all other options in the default configuration on this interface.

PCI Express X8(Port0)		
PCI Express X8(Port0)	<Enabled>	Control the PCI Express Root Port.
PCIe Bandwidth	<X4>	
PCIe Max Speed	<Gen4>	
ASPM Max Support	<L0sL1>	
ASPM	<Disable>	
Max Payload Support	<512 Bytes>	
DTI Support	<Disabled>	

In addition, other PCIE Root Port 1-4 can be operated by referring to the PCIE Root Port 0 option interface.

3.6.6. USB Configuration

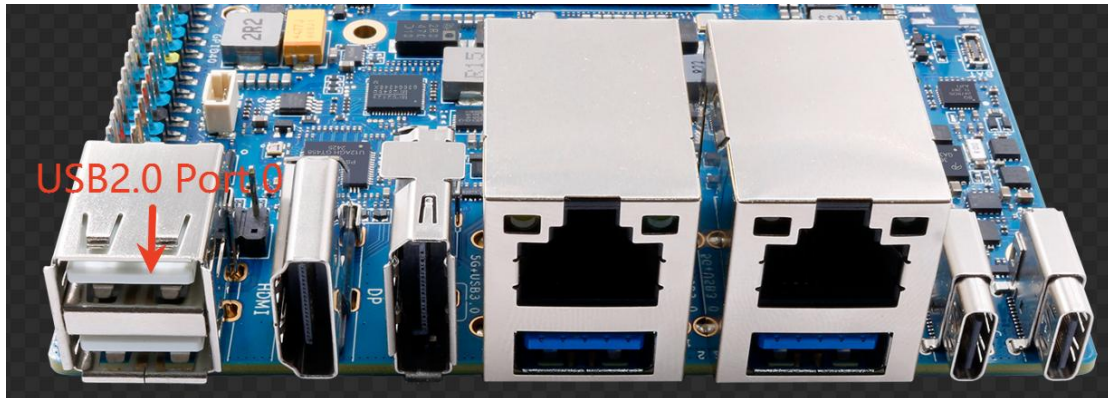
This interface is used to control the USB2.0/USB3.0/USBC enable switch.

USB Configuration		
USB2 Controller 0	<Enabled>	USB 2.0 Controller Enable/Disable
USB2 Controller 1	<Enabled>	
USB2 Controller 2	<Enabled>	
USB2 Controller 3	<Enabled>	
USB3 Controller 0	<Enabled>	
USB3 Controller 1	<Enabled>	
USBC DRD Controller	<Enabled>	
USBC DRD Controller Role	<Host>	
USBC Controller 0	<Enabled>	
USBC Controller 1	<Enabled>	
USBC Controller 2	<Enabled>	

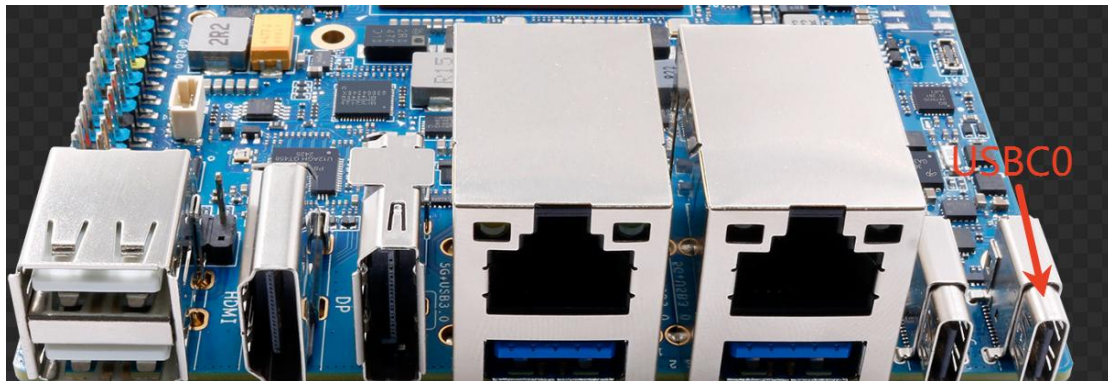
^v=Move Highlight	F9=Reset to Defaults <Enter>=Select Entry	F10=Save Esc=Exit
-------------------	--	----------------------



USB2 Controller 0: When the option is enabled, enable the USB2.0 port0; When the option is disabled, close the USB2.0 port0.



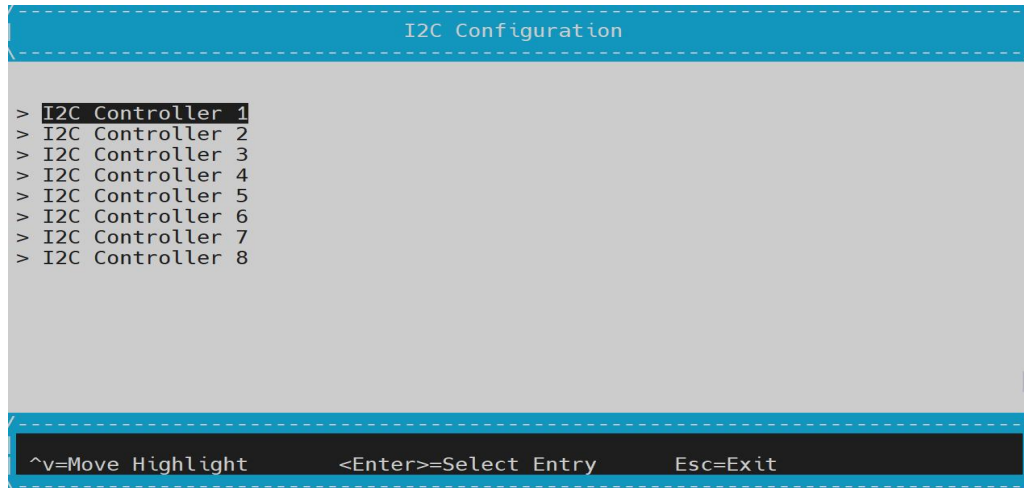
USBC DRD Controller Role: When the option is Host, USBC0 serves as the Host function, responsible for discovering devices, allocating resources, controlling communication, and managing power; When the option is Devcie, USBC0 serves as the Devcie function and passively responds to the Host's request.



In addition, other USB ports such as 1/2/3 can refer to the USB Port 0 option interface for operation.

3.6.7. I2C Configuration

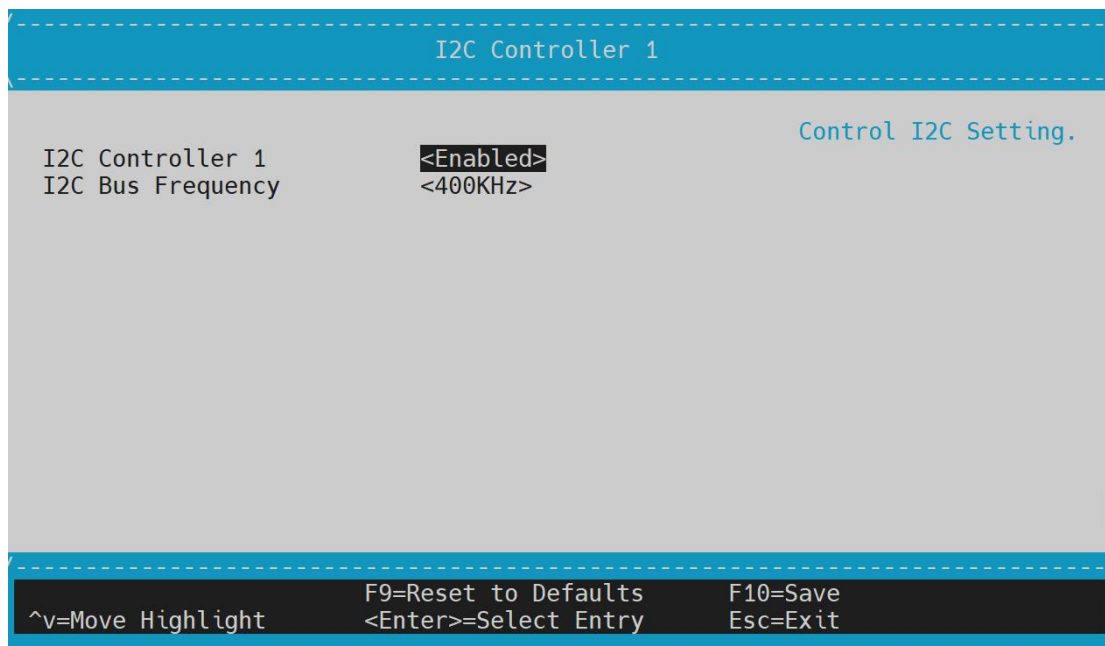
This interface is used to control the enable switch options for I2C1-I2C8.



I2C controller 1:Enable I2C0 port when option is enabled;

When the option is Disabled, close the I2C0 port.

I2C Bus frequency :When the option is 400kHz, the frequency is set to 400kHz

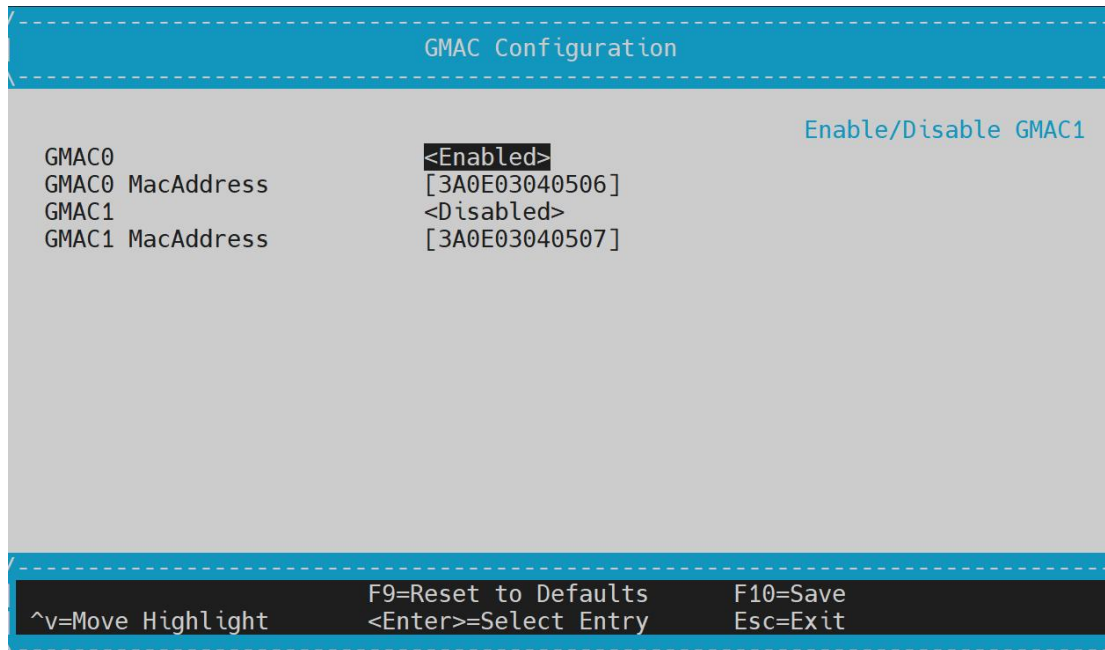


In addition, other I2C ports 2-8 can refer to the I2C Port 1 option for operation

3.6.8. GMAC Configuration

This interface is used to control the enable switch options for GMAC.

The development board currently does not support GMAC, so this part can be temporarily ignored



3.6.9. Platform Configuration

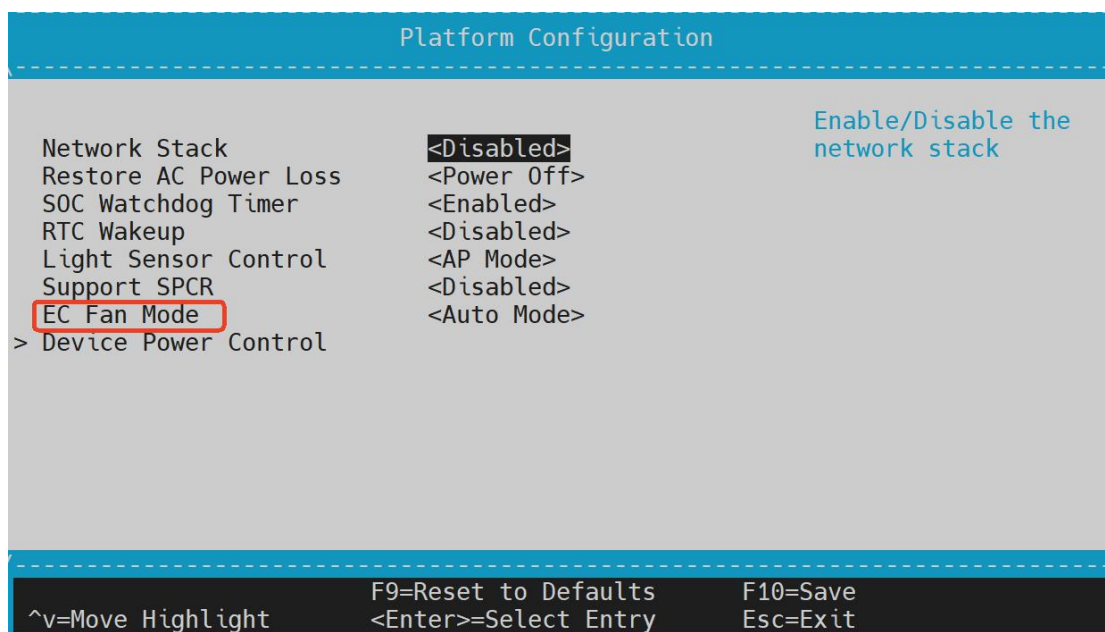
This interface is a platform related option control switch.

For example, EC Fan mode

When selecting Auto Mode mode, the fan speed increases as the CPU temperature rises;

When selected as Performance Mode mode, the fan will run at duty 100% speed.

Attention: Except for the EC Fan mode option, please maintain the default configuration on this interface and modify it with caution.

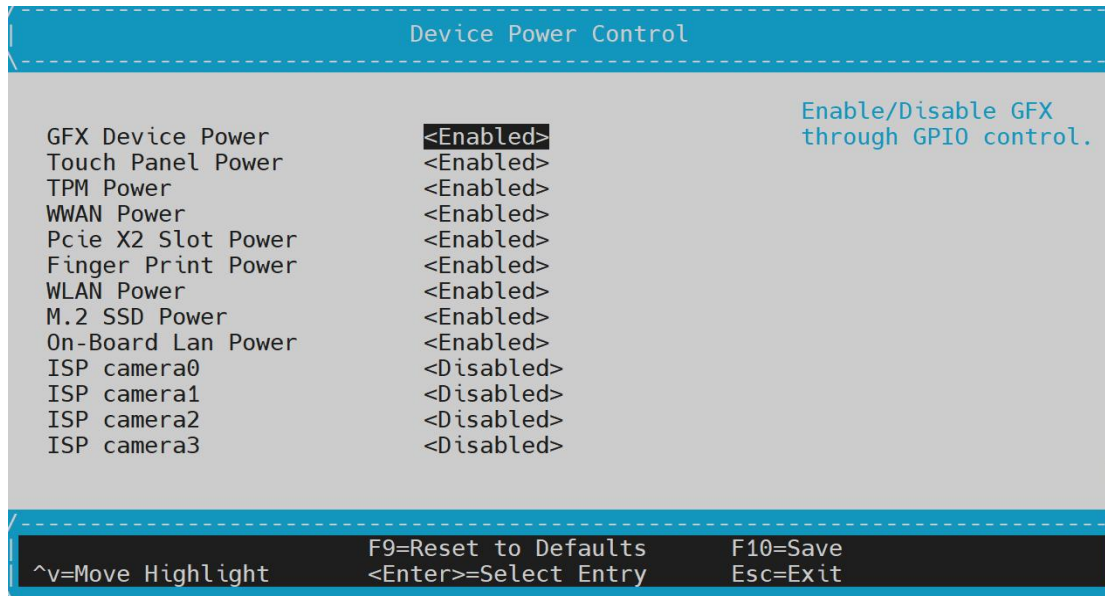




3.6.10. Device Power Control

This interface enables GPIO control switches for some devices.

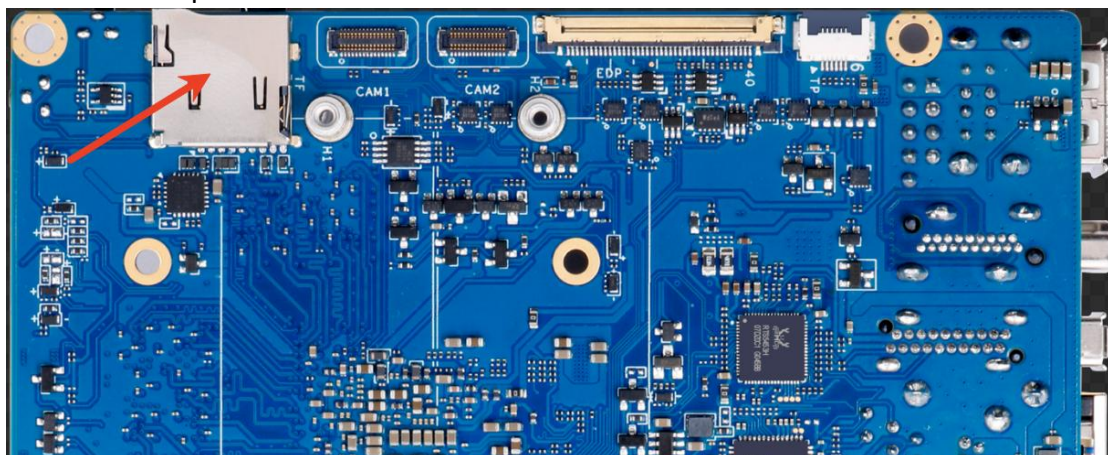
This section is for the purpose of enabling equipment power supply. It is recommended to modify it carefully, otherwise it may cause equipment failure or loss



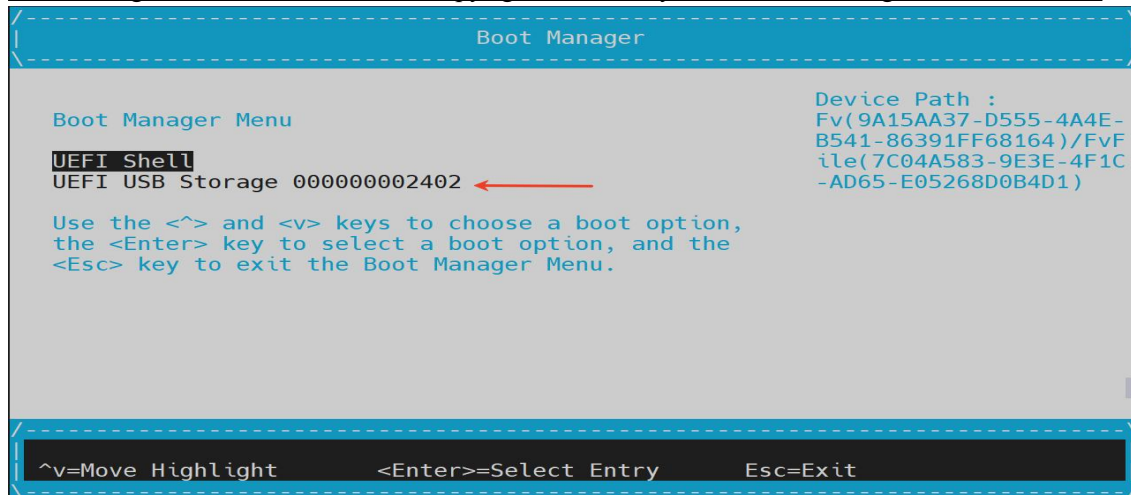
3.7 Boot Manager

3.7.1 TF card recognition

1) The development board has an SD card slot as follows

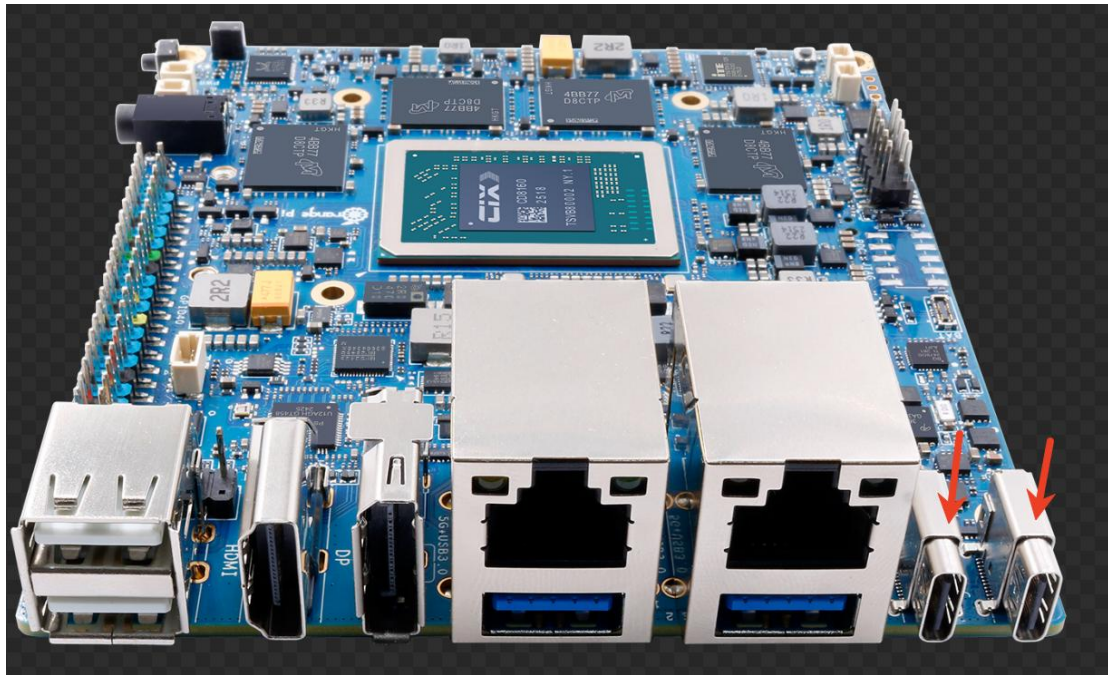


2) Connect the TF card to the card slot, power on the board, and the TF card can be recognized

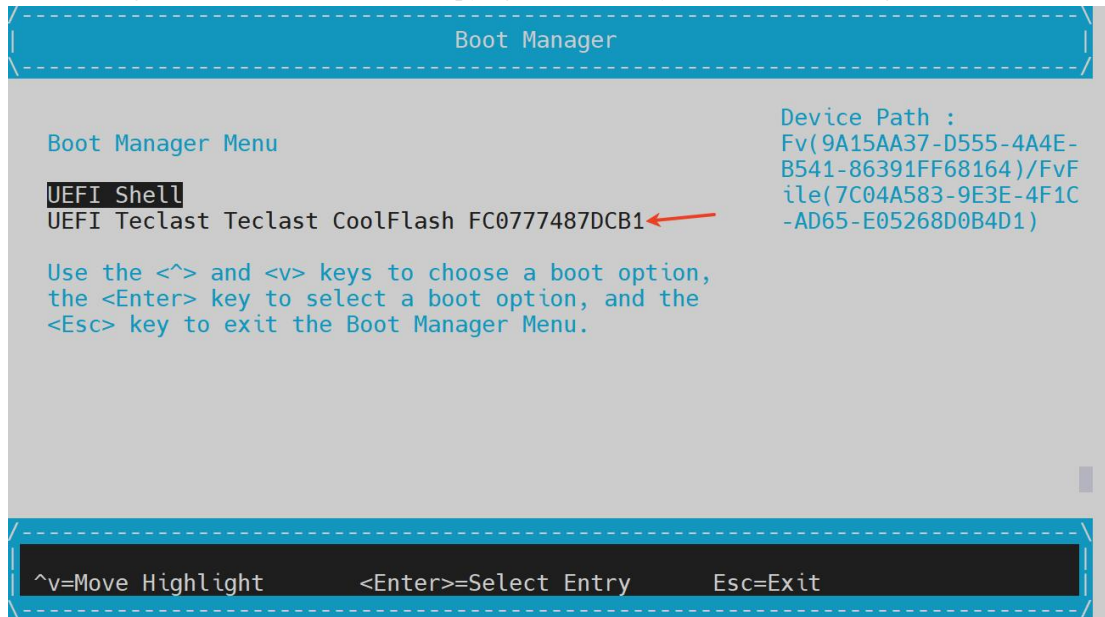


3.7.2 Typec3.0 recognition

1) The development board has 2 Typec interfaces as follows

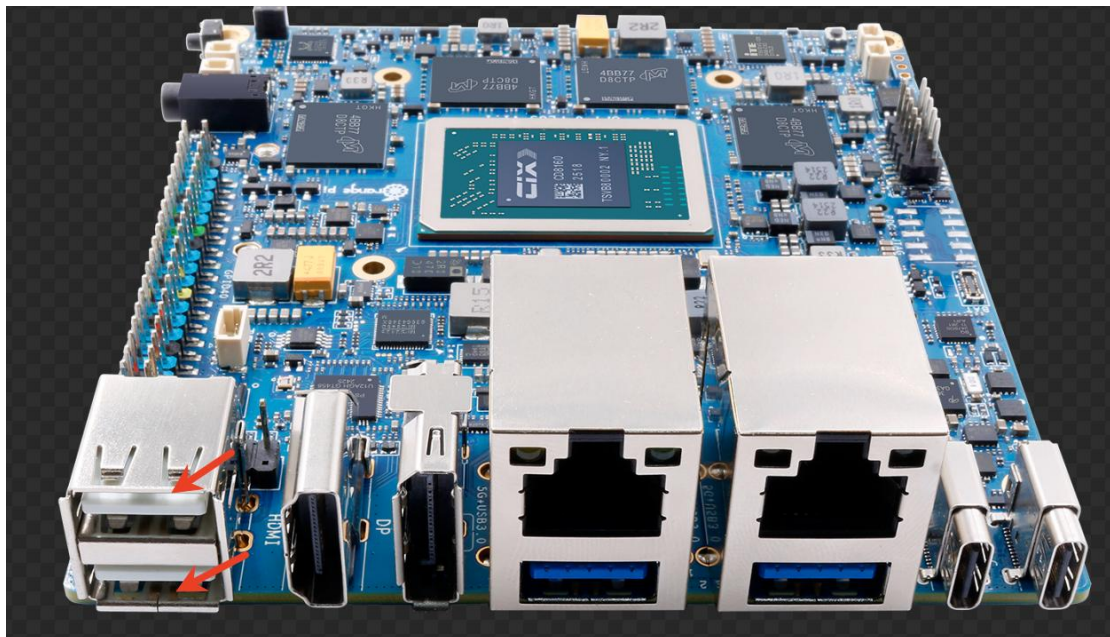


2) Connect the USB3.0 USB flash drive with Typec interface, power on the board, and recognize the USB flash drive normally



3.7.3 USB 2.0 recognition

1) The development board has 2 USB 2.0 interfaces as follows



2) 2) Insert a USB flash drive into the USB 2.0 port and power on the development board to recognize the USB flash drive.



Boot Manager

Boot Manager Menu

Windows Boot Manager

UEFI Shell

UEFI KINGSTON OM8SEP4512Q-A0 50026B7381956BD9 1

UEFI Kingston DataTraveler 3.0
408D5C15AFB8E720F9040050UEFI Kingston DataTraveler 3.0
E0D55E6CE778184198490A20

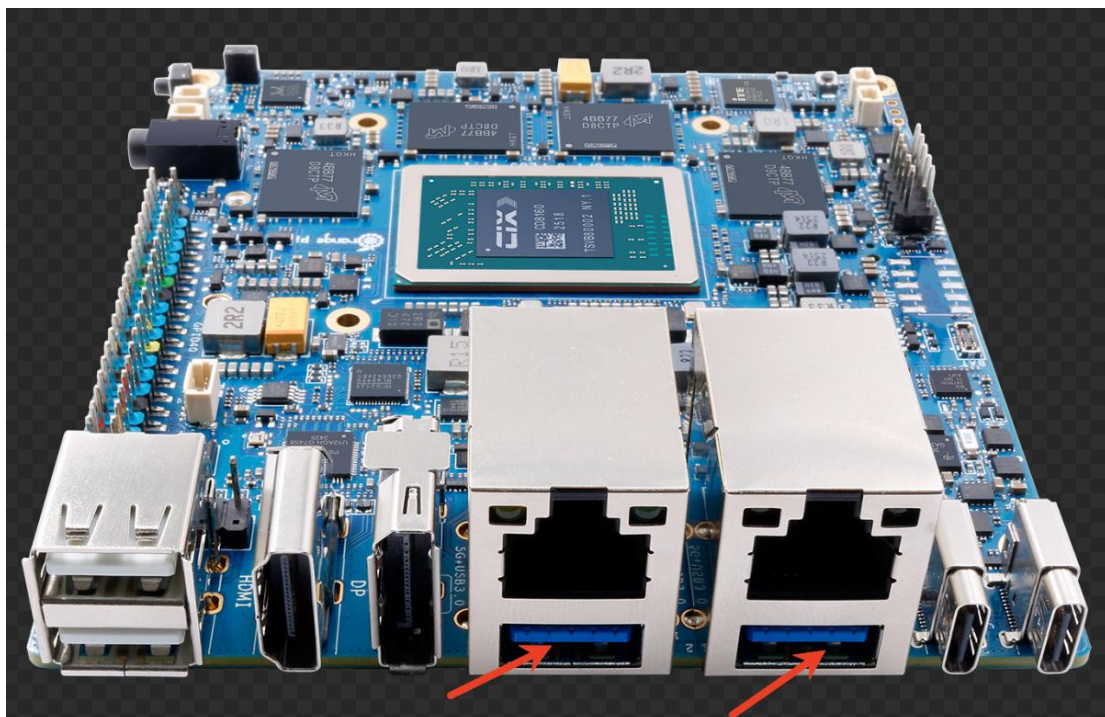
Device Path :

Fv(9A15AA37-D555-4A4E-B541-86391FF68164)/FvFile(7C04A583-9E3E-4F1C-AD65-E05268D0B4D1)

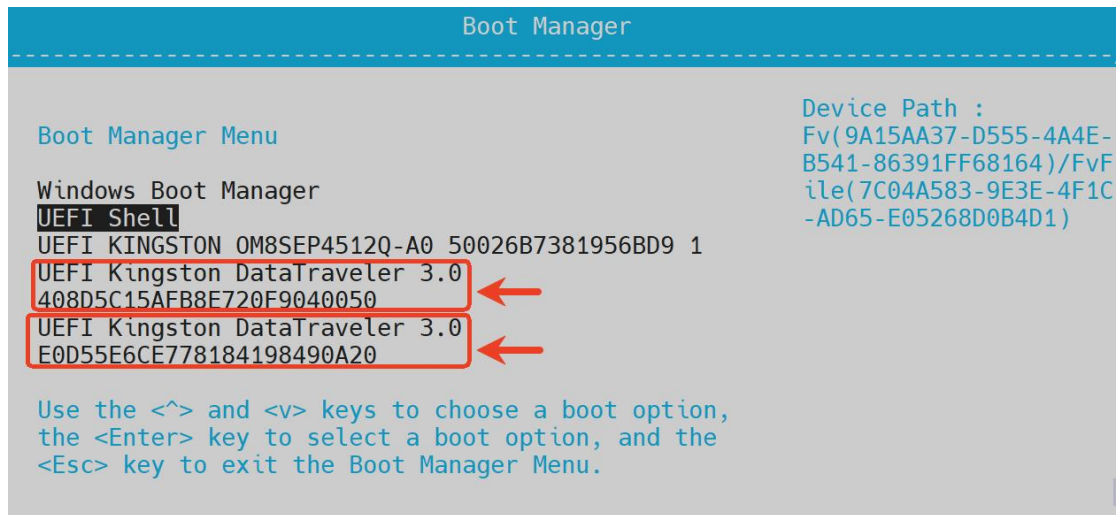
Use the <^> and <v> keys to choose a boot option,
the <Enter> key to select a boot option, and the
<Esc> key to exit the Boot Manager Menu.

3.7.4 USB 3.0 recognition

1) The development board has 2 USB3.0 interfaces as follows

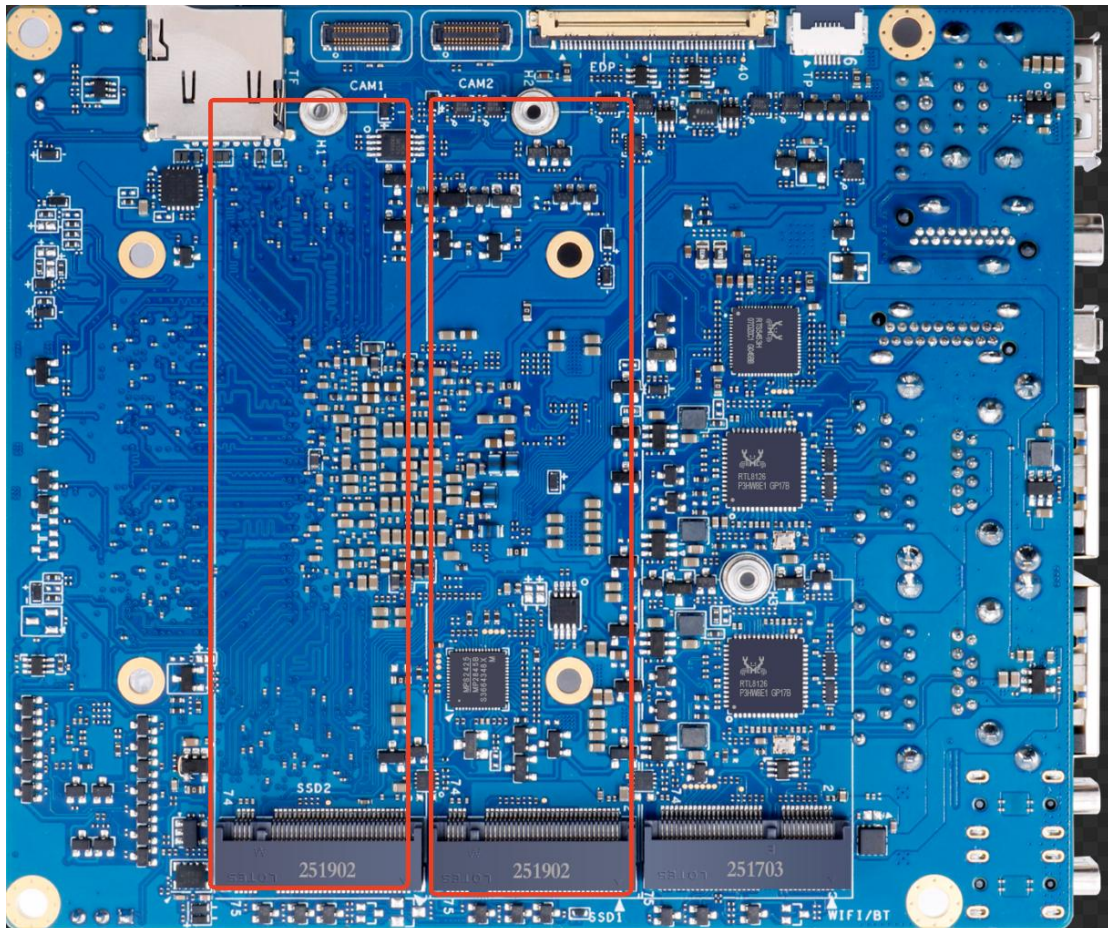


2) Insert a USB flash drive into the USB 3.0 port and power on the development board to recognize the USB flash drive.

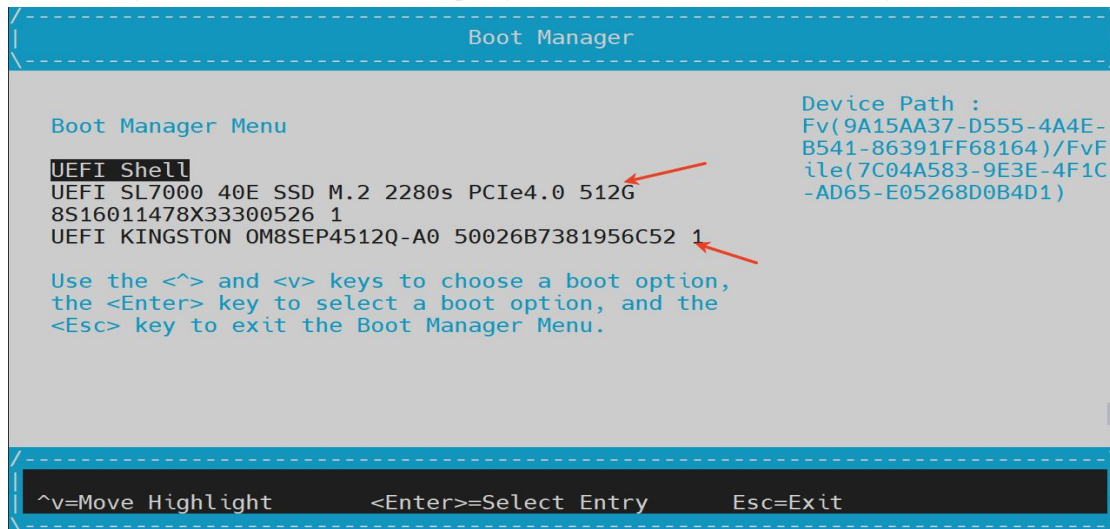


3.7.4 SSD hard drive recognition

1) The development board has 2 SSD PCIE interfaces as follows



1) Both SSD1 and SSD2 slots are connected to SSD hard drives (one Lenovo SSD and one Kingston SSD), power on the board, and recognize SSD hard drives normally



4.USB flash drive burning Bios

4.1 Creating a shell Disk

1) Prepare a USB flash drive in fat32 format and copy bios bin, FlashUpdate.efi, and EFI environment.

Regarding the creation of FAT32 formatted USB drives:

You can find similar tools such as DiskGenius online to implement it

For example: <https://www.diskgenius.cn/download.php>

2) The following is a DiskGenius diagram for reference:

Select the USB drive, format the current partition, choose FAT32 file system, and click the format button





4.2 BIOS acquisition

A. Visit the official website

<http://www.orangepi.cn/html/hardWare/computerAndMicrocontrollers/service-and-support/Orange-Pi-6-Plus.html>

B. Click on the "BIOS" icon on the official website page to enter

C. Find the BIOS firmware release package

D. There are two types of BIOS in the BIOS firmware release package:

[1] AndroidBIOS:

BIOS dedicated to Android system

[2] GeneralBIOS:

Suitable for systems such as Debian Linux, OpenHarmony, Windows 11 ARM64, etc BIOS;

E. Place EFI in the root directory of a FAT32 formatted USB drive, 在 FAT32

F. You can also place opi_6plus_flash in the root directory of the USB drive

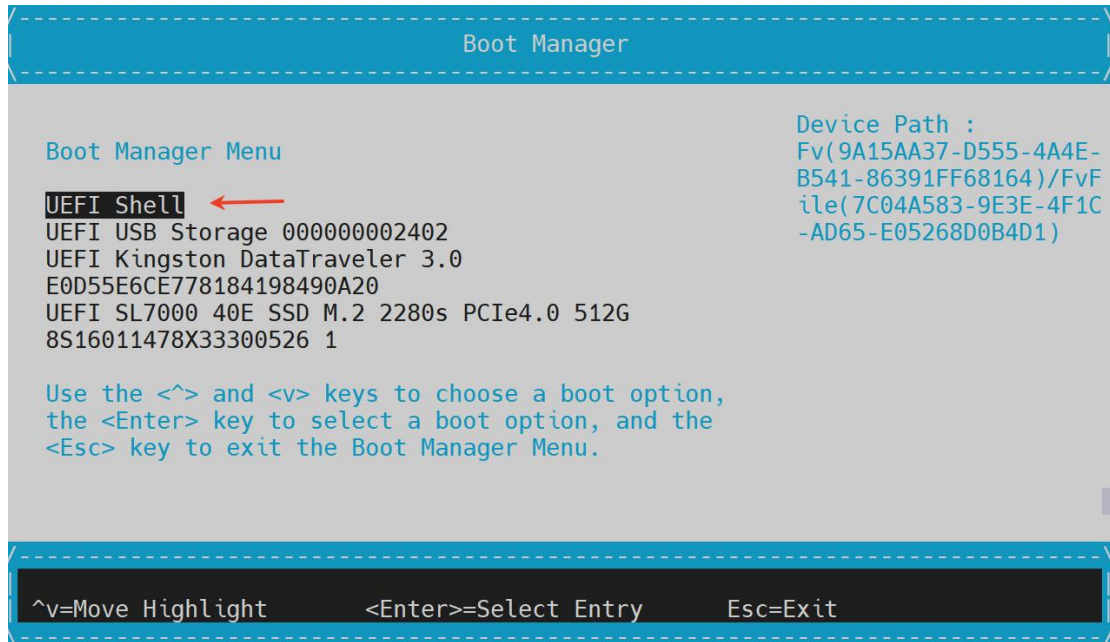
G. Please refer to the following 2) BIOS burning chapter for the burning steps

4.3 Burn bios

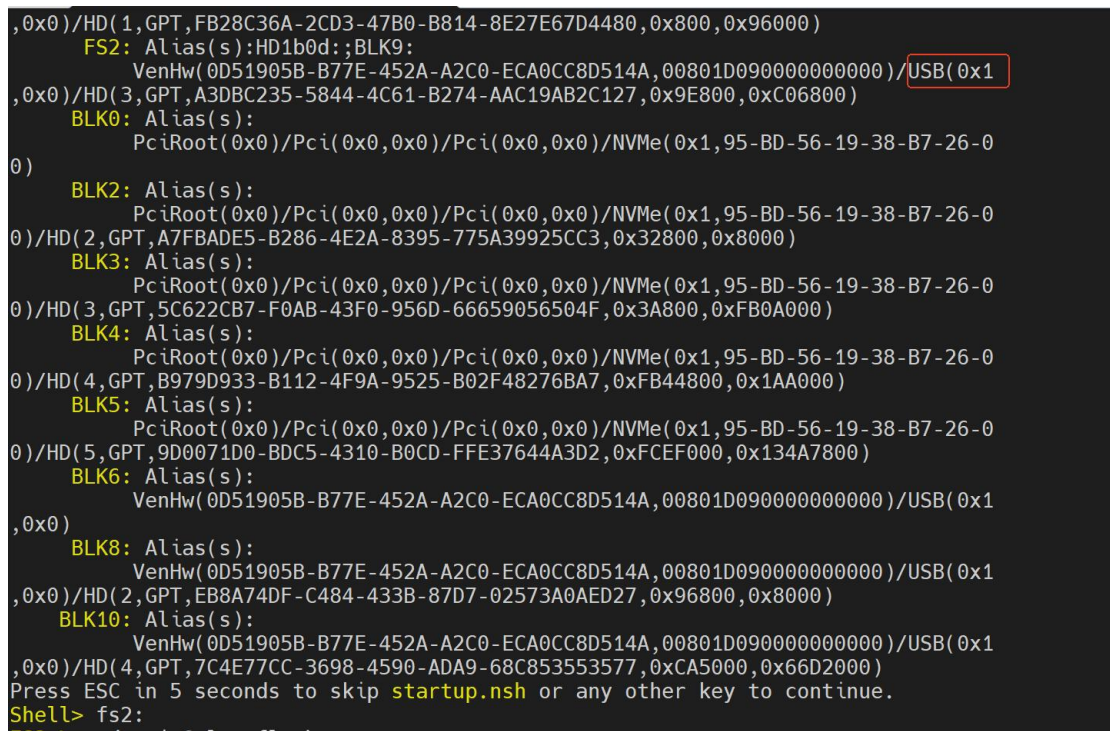
1) Power on the board, press the F2/ESC shortcut key to enter BIOS, and select "Boot Manager" to enter.



2) Click on UEFI Shell



Enter the shell and select your own USB drive to enter. Here is fs2, but it may actually be FS0, FS1, etc. You need to enter according to the actual situation. The 'ls' command can view the current directory and confirm that a USB drive has been entered 入 shell



3) Enter the opi_6plus_flash directory and execute the burn command 入
opi_6plus_flash

FlashUpdate.efi -f OPI6PLUS_BIOS_1.0_General.bin



```
FS2:\> cd opi_6plus_flash
FS2:\opi_6plus_flash> ls
Directory of: FS2:\opi_6plus_flash\
10/16/2025  13:51 <DIR>          4,096  .
10/16/2025  13:51 <DIR>           0     ..
02/18/2025  14:28                434,176  FlashUpdate.efi
10/16/2025  11:30                6,288,078  OPI6PLUS_BIOS_1.0_Android.bin
10/16/2025  11:31                6,288,078  OPI6PLUS_BIOS_1.0_General.bin
10/16/2025  11:30                6,288,078  OPI6PLUS_BIOS_1.0_OpenHarmony.bin
               4 File(s)  19,298,410 bytes
               2 Dir(s)
FS2:\opi_6plus_flash> FlashUpdate.efi -f OPI6PLUS_BIOS_1.0_General.bin
```

4.4 Burning situation

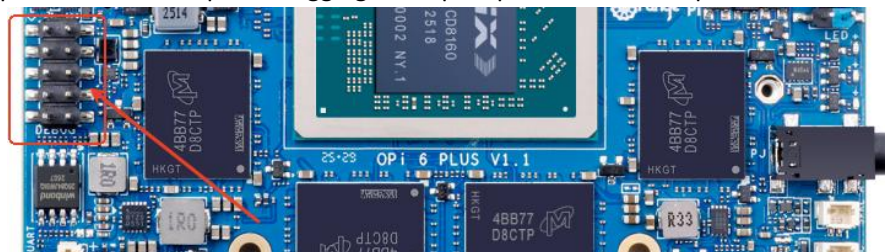
After burning the BIOS program, the board will restart.

```
Shell> fs2:
FS2:\> cd opi_6plus_flash
FS2:\opi_6plus_flash> FlashUpdate.efi -f OPI6PLUS_BIOS_1.0_General.bin
=====
Copyright 2024 Cix Technology Group Co., Ltd. All Rights Reserved.
FlashUpdate Utility v1.04.
Build Date:Jan 23 2025
=====
Old Verison:BiosV1.0-W20251016
New Verison:BiosV1.0-W20251016
[00.13] Processing...
Flash update success.
System will be reset...
```

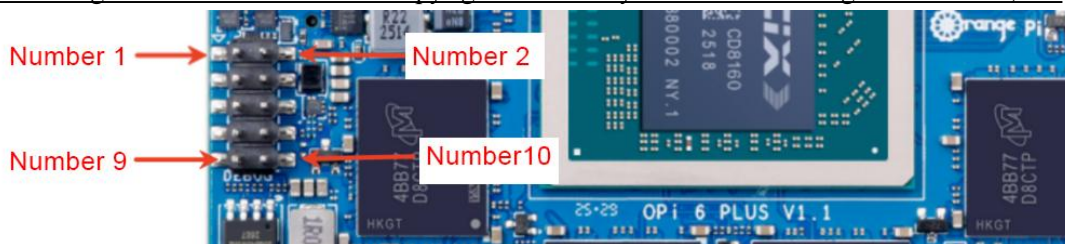
5.How to use 10pin to debug serial port

5.1 10 pin debugging serial port pin instructions

The position of the 10 pin debugging serial port pin on the development board is as follows:



The definition of the serial port pin number for 10 pin debugging is as follows:



The function of each pin in the 10pin debugging serial port can be found in the following table. **Generally speaking, normal use of the development board only requires the use of the UART2 debugging serial port, and other debugging serial ports do not need to be paid attention to and are basically not needed.**

Default function	Pin function	Serial number	Serial number	Pin function	Default function
BIOS and kernel logs	UART2_TX	1	2	UART4_TX	PM log
	UART2_RX	3	4	UART4_RX	
	GND	5	6	GND	
Post code log	UART6_TX	7	8	UART5_TX	SE log
	UART6_RX	9	10	UART5_RX	

5.2 Connection instructions for debugging serial ports corresponding to BIOS and kernel

1) Firstly, it is necessary to prepare a **3.3V** USB to TTL module, and then plug one end of the USB interface of the USB to TTL module into the USB interface of the computer.。



The 5V of the USB to TTL module does not need to be connected

The jumper cap of the USB to TTL module needs to be connected

The TXD of the USB to TTL module is connected to the RXD of the debugging serial port of the development board

The RXD of the USB to TTL module is connected to the TXD of the debugging serial port of the development board

The GND of the USB to TTL module is connected to the GND of the debugging serial port of the development board

2) The development board defaults to using UART2 to output BIOS and kernel logs. The positions of the UART debugging serial GND, RXD, and TXD pins are shown in the following figure:





3) The GND, TXD, and RXD pins of the USB to TTL module need to be connected to the UART2 debugging serial port on the development board through DuPont wires.

- a. Connect the GND of the USB to TTL module to the GND of the development board
- b. **Connect the RX of the USB to TTL module to the UART2-TX pin** on the development board
- c. **Connect the TX of the USB to TTL module to the UART2-RX pin** on the development board

4) The schematic diagram of connecting a USB to TTL module to a computer and Orange Pi development board is shown below



Schematic diagram of connecting the USB to TTL module to the computer and the Orange Pi development board

The TX and RX of the serial port need to be cross connected. If you don't want to carefully distinguish the order of TX and RX, you can randomly connect the TX and RX of the serial port first. If there is no output during testing, then switch the order of TX and RX. This way, there will always be a correct order.



6. Appendix

6.1 User manual update history

Version	Date	Update Notes
v1.0	2025-10-15	Initial version

6.2 BIOS firmware update history

Date	Update Notes
2025-10-15	OPI6PLUS_BIOS_1.0_Android.bin、OPI6PLUS_BIOS_1.0_General.bin * Initial version